F18A VDP REGISTERS (VR)

The 9918A and F18A have a 14-bit address counter and TI numbers the MS-bit as zero. Address bits are A0..A13, data bits are D0..D7.

Same as 9918A	F18A Only
Different from 9918A	F18A Ignores - reserved 0

Register	0 MSbit	1	2	3	4	5	6	7 LSbit	
									Mode = M4 M3 M2 M1
									GM1 = 0 0 0 0
									GM2 = 0 1 0 0
VR0 >00	0	0	0	IE1	0	M4	M3	ExtVid	MCM = 0 0 1 0
									TXT1 = 0 0 0 1 (40 col)
VR1 >01	4K/16K	BLANK	IE0	M1	M2	0	SIZE	MAG	TXT2 = 1 0 0 1 (80 col)
VR2 >02	0	0	0	0	A0	A1	A2	A3	Name Table Base Address, 1K boundaries
									768-bytes per table for 24 rows
									960-bytes per table for 30 rows
VR3 >03	A0	A1	A2	A3	A4	A5	A6	A7	Color Table Base Address, 64-byte boundaries
									32-bytes for normal mode
									256-bytes for enhanced color mode
									Color Table becomes Tile Attribute Table Base Address and goes from 32 to 256 bytes long
									768 to 4K when in position-attribute mode depending on the size of the horz / vert pages.
VR4 >04	0	0	0	0	0	A0	A1	A2	Pattern Generator Base Address, 2K boundaries
									2K for 256 tiles
									4K for 2-bit color mode, 6K for 3-bit color mode
VR5 >05	0	A0	A1	A2	A3	A4	A5	A6	Sprite Attribute Table Base Address, 128-byte boundaries
									128-bytes (32 sprites, 4 bytes each)
VR6 >06	0	0	0	0	0	A0	A1	A2	Sprite Pattern Generator Base Address, 2K boundaries
									2K for 256 patterns
									4K for 2-bit color mode, 6K for 3-bit color mode
VR7 >07	FG0	FG1	FG2	FG3	BG0	BG1	BG2	BG3	Text color / background color
VR10 >0A	0	0	0	0	A0	A1	A2	A3	Name Table 2 Base Address, 1K boundaries
									768-bytes per table for 24 rows
									960-bytes per table for 30 rows
VR11 >0B	A0	A1	A2	A3	A4	A5	A6	A7	Color Table 2 Base Address, 64-byte boundaries
									32-bytes for normal mode
									256-bytes for enhanced color mode
									Color Table becomes Tile Attribute Table Base Address and goes from 32 to 256 bytes long
									768 to 4K when in position-attribute mode depending on the size of the horz / vert pages.
VR15 >0F	0	CNT_RESET	CNT_SNAP	CNT_START	S0	S1	S2	S3	Status Reg number to read
									counter: reset: 1 = reset, start/stop: 1 = start, 0 = stop, snap = 1 snapshot the counter without stopping
VR19 >13	IL0	IL1	IL2	IL3	IL4	IL5	IL6	IL7	Horz interrupt scan line, 0 to disable
VR24 >18	0	0	SPS0	SPS1	T2PS0	T2PS1	T1PS0	T1PS1	Sprite Palette Select two-MSBs in normal mode
									Tile Palette Select two-MSBs in normal mode
VR25 >19	HTO0	HTO1	HTO2	HTO3	HTO4	HPO0	HPO1	HPO2	Horizontal tile and pixel offset 2

VR26 >1A	VTO0	VTO1	VTO2	VTO3	VTO4	VPO0	VPO1	VPO2	Vertical tile and pixel offset 2
VR27 >1B	HTO0	HTO1	HTO2	HTO3	HTO4	HPO0	HPO1	HPO2	Horizontal tile and pixel offset
VR28 >1C	VTO0	VTO1	VTO2	VTO3	VTO4	VPO0	VPO1	VPO2	Vertical tile and pixel offset
VR29 >1D	SPGS0	SPGS1	HPSIZE2	VPSIZE2	TPGS0	TPGS1	HPSIZE1	VPSIZE1	HPSIZE = horizontal page size, 0 = 1 page, 1 = 2 pages
									VPSIZE = vertical page size, 0 = 1 page, 1 = 2 pages
									SPGS = sprite pattern generator offset size, 11=256, 10=512, 01=1K, 00=2K
									TPGS = tile pattern generator offset size, 11=256, 10=512, 01=1K, 00=2K
VR30 >1E	0	0	0	SPRTMAX0	SPRTMAX1	SPRTMAX2	SPRTMAX3	SPRTMAX4	SPRTMAX0..4 = Max sprites per scan line, set to 0 to reset sprite max to jumper setting
VR31 >1F	BML_EN	BML_PRI	BML_TRANS	BML_FAT	BMLPS0	BMLPS1	BMLPS2	BMLPS3	BML: Enable, Priority over sprites, Transparent, Fat pixels, Palette select
VR32 >20	BMLBA0	BMLBA1	BMLBA2	BMLBA3	BMLBA4	BMLBA5	BMLBA6	BMLBA7	Bitmap Layer Base Address, 64-byte boundaries
VR33 >21	BMLX0	BMLX1	BMLX2	BMLX3	BMLX4	BMLX5	BMLX6	BMLX7	Bitmap x
VR34 >22	BMLY0	BMLY1	BMLY2	BMLY3	BMLY4	BMLY5	BMLY6	BMLY7	Bitmap y
VR35 >23	BMLW0	BMLW1	BMLW2	BMLW3	BMLW4	BMLW5	BMLW6	BMLW7	Bitmap width
VR36 >24	BMLH0	BMLH1	BMLH2	BMLH3	BMLH4	BMLH5	BMLH6	BMLH7	Bitmap height
VR47 >2F	DPM	AUTO INC	PR0	PR1	PR2	PR3	PR4	PR5	DPM = data-port mode
									AUTO INC = auto inc palette index after each write
									Palette register #
VR48 >30	SIGN-BIT	INC0	INC1	INC2	INC3	INC4	INC5	INC6	SIGNED two's-complement increment amount for VRAM address, defaults to 1
VR49 >31	TILE2_EN	ROW30	ECMT0	ECMT1	Y_REAL	LINK	ECMS0	ECMS1	ECM = enhanced color mode, (T)ile and (S)prite
	Tile Map 2 enable		ECM (T)ile		real sprite Y coord		ECM (S)prite		0=nomal
		24 / 30 tile rows				Sprite Linking enable			1=1-bit color mode, tile attributes
									2=2-bit color mode, tile attributes
									3=3-bit color mode, tile attributes
VR50 >32	VR_RESET	GPU_HTRIG	GPU_VTRIG	TL1_OFF	RPTMAX	SCANLINES	POS_ATTR	TILE2_PRI	0 = TL2 always on top, 1 = TL2 vs sprite priority is considered
							position vs name attribute		0 = per name attributes in ECMs, 1 = per position attributes
						show virtual scan lines			0 = no virtual scan lines, 1 = enable virtual scan lines
					report sprite max vs 5th sprite				0 = report 5th sprite, 1 = report max sprite (VR30)
				Disable all tile 1 layers					0 = normal, 1 = disable GM1, GM2, MCM, T40, T80
			GPU vsync trig						0 = disable, 1 = trigger GPU on VSYNC
		GPU hsync trig							0 = disable, 1 = trigger GPU on HSYNC
	Reset VDP registers								0 = ignored, 1 = reset all VDP registers to power-on defaults
VR51 >33	0	0	STOPSPRT0	STOPSPRT1	STOPSPRT2	STOPSPRT3	STOPSPRT4	STOPSPRT5	Stop Sprite to limit the total number of sprites to process, defaults to 32
VR54 >36	GPU0	GPU1	GPU2	GPU3	GPU4	GPU5	GPU6	GPU7	GPU address MSB
VR55 >37	GPU8	GPU9	GPU10	GPU11	GPU12	GPU13	GPU14	GPU15	GPU address LSB, writing resets and loads, then triggers the GPU
VR56 >38	0	0	0	0	0	0	0	GPU OP	GPU Operation performed when register is written:
									0 = reset and load PC, 1 = trigger GPU to begin execution
VR57 >39	0	0	0	1	1	1	0	0	Enable registers over 7, write 000111xx to VR57 twice
VR58 >3A	0	0	0	0	GCLK0	GCLK1	GCLK2	GCLK3	GROM Clock half-period counter, 6 (min) to F = 6F to FF
F18A STATUS REGISTERS (SR)									
SR0	F	5S	C	SP0	SP1	SP2	SP3	SP4	
SR1	ID0	ID1	ID2	0	0	0	BLANKING	HF	ID = >00 for 9938, >40 (010xxxxx) for 9958

									ID = >E0 (111xxxxx) for F18A
									HF = 1 when scan line == R19, if R19 != 0
									BLANKING = 1 during horz or vert blanking periods
SR2	GPU ST	GDATA0	GDATA1	GDATA2	GDATA3	GDATA4	GDATA5	GDATA6	GPU Status: 1 = running, 0 = idle
									GPU Data: 7-bits of user programmable data from the GPU
SR3	SCANLINE0	SCANLINE1	SCANLINE2	SCANLINE3	SCANLINE4	SCANLINE5	SCANLINE6	SCANLINE7	Current scan line, 0 when not in active area
SR4	NANO2	NANO3	NANO4	NANO5	NANO6	NANO7	NANO8	NANO9	Nanosecond counter (0..999) LSB
SR5	0	0	0	0	0	0	NANO0	NANO1	Nanosecond counter (0..999) MSB
SR6	MICRO2	MICRO3	MICRO4	MICRO5	MICRO6	MICRO7	MICRO8	MICRO9	Microsecond counter (0..999) LSB
SR7	0	0	0	0	0	0	MICRO0	MICRO1	Microsecond counter (0..999) MSB
SR8	MILLI2	MILLI3	MILLI4	MILLI5	MILLI6	MILLI7	MILLI8	MILLI9	Millisecond counter (0..999) LSB
SR9	0	0	0	0	0	0	MILLI0	MILLI1	Millisecond counter (0..999) MSB
SR10	SECOND8	SECOND9	SECOND10	SECOND11	SECOND12	SECOND13	SECOND14	SECOND15	Second counter (0..65535) LSB
SR11	SECOND0	SECOND1	SECOND2	SECOND3	SECOND4	SECOND5	SECOND6	SECOND7	Second counter (0..65535) MSB
SR12	Unused								
SR13	Unused								
SR14	VMAJOR0	VMAJOR1	VMAJOR2	VMAJOR3	VMINOR0	VMINOR1	VMINOR2	VMINOR3	Major/Minor version, 00010011 = v1.3
SR15	READ0	READ1	READ2	READ3	READ4	READ5	READ6	READ7	VDP read register value (see VR15). Updated any time a VRAM address is set

Sprite attribute byte when F18A is locked (compatible with original VDP)

ECLK	0	0	0	COL0	COL1	COL2	COL3	

Sprite attribute byte when F18A is unlocked, all modes and ECM settings

ECLK	FLIP X	FLIP Y	SIZE	PS0	PS1	PS2	PS3	Size: 0 = global setting, 1 = 16x16

Sprite Linking, link table follows SAT and adds 32 bytes to the SAT table size

0	0	LINK	PARENT0	PARENT1	PARENT2	PARENT3	PARENT4	Linking is only 1 level
								LINK, when 1, PARENT points to sprite's parent
								PARENT = sprite name of parent

Tile attribute byte in Enhanced Color Modes

Color Table becomes Tile Attribute Table Base Address and goes from 32 to 256 or 2K (same as name table) bytes long

PRI	FLIP X	FLIP Y	TRANS	PS0	PS1	PS2	PS3	PRI = priority over sprites
								TRANS = when 1, colors with 0, 00 or 000 will be transparent instead of a palette index

When T40/T80 Mode, ECM0, and Position-Based Attributes is Enabled

FG0	FG1	FG2	FG3	BG0	BG1	BG2	BG3	T40/T80 fg / bg color

F18A GPU NEW AND MODIFIED INSTRUCTION SUMMARY

Instruction	Opcode	Addressing		New name	
CALL	>0C80	0000 1100 10Ts SSSS	new	CALL	Call subroutine, push return address on stack
RET	>0C00	0000 1100 0000 0000	new	RET	Return from subroutine, pop return address from stack
PUSH	>0D00	0000 1101 00Ts SSSS	new	PUSH	Push a 16-bit word onto the stack
POP	>0F00	0000 1111 00Td DDDD	new	POP	Pop a 16-bit word off of the stack
SLC	>0E00	0000 1110 00Ts SSSS	new	SLC	Shift Left Circular
CKON	>03A0		modified	SPI_EN	Sets the chip enable line to the SPI Flash ROM low (enables the ROM)
CKOF	>03C0		modified	SPI_DS	Sets the chip enable line to the SPI Flash ROM high (disables the ROM)
IDLE	>0340		modified	IDLE	Forces the GPU state machine to the idle state, restart with VR56 trigger
LDCR	>3000		modified	SPI_OUT	Writes a byte (always a byte operation) to the SPI Flash ROM

STCR	>3400			modified	SPI_IN				Reads a byte (always a byte operation) from the SPI Flash ROM	
RTWP	>0380			modified	RTWP				Does not use R13, only performs R14->PC, R15->status flags	
XOP	>2C00			modified	PIX				New dedicated pixel plotting and addressing instruction	
UNIMPLEMENTED INSTRUCTIONS										
SBO										
SBZ										
TB										
BLWP										
STWP										
LWPI										
LIMI										
RSET										
LREX										