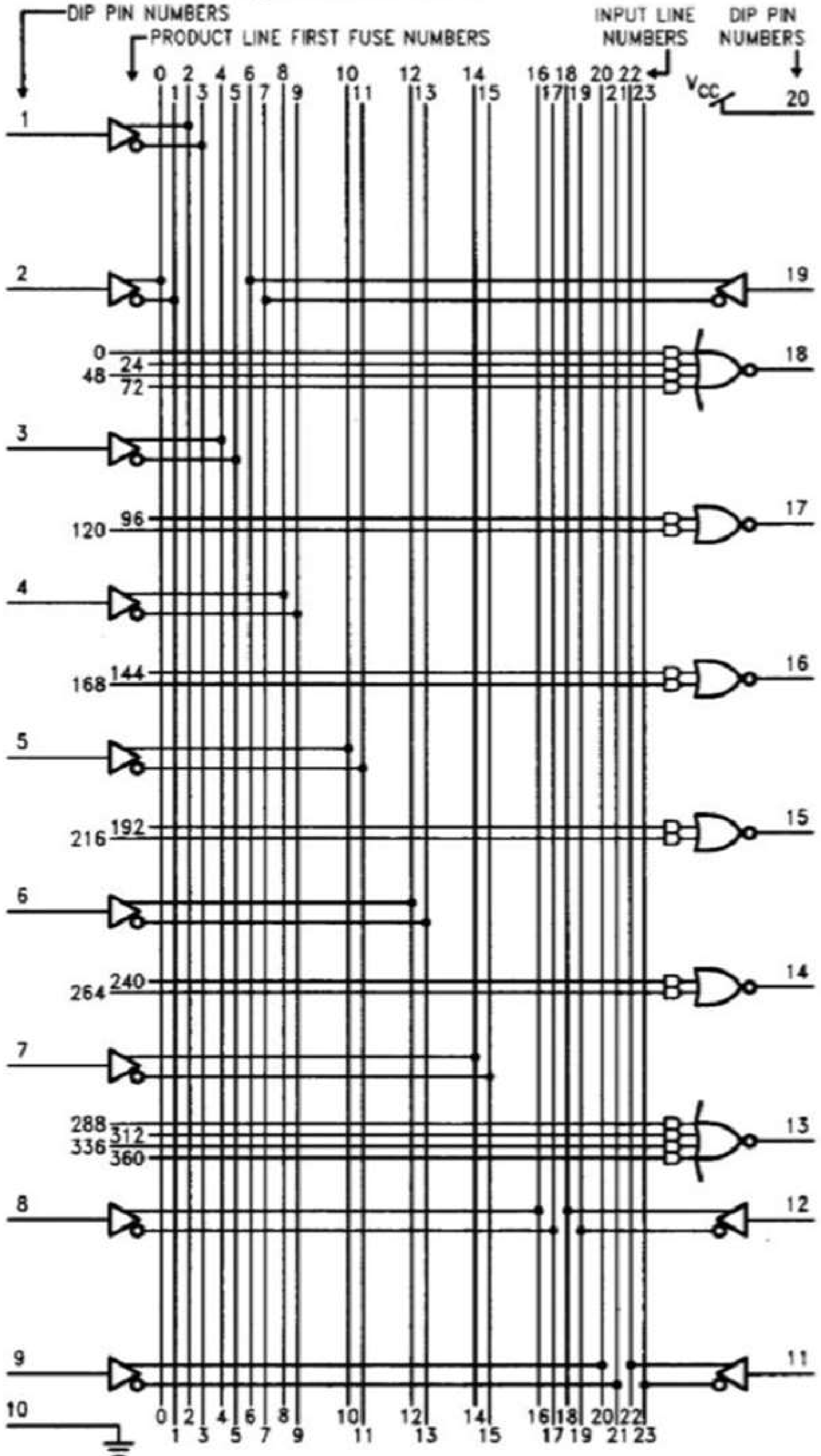
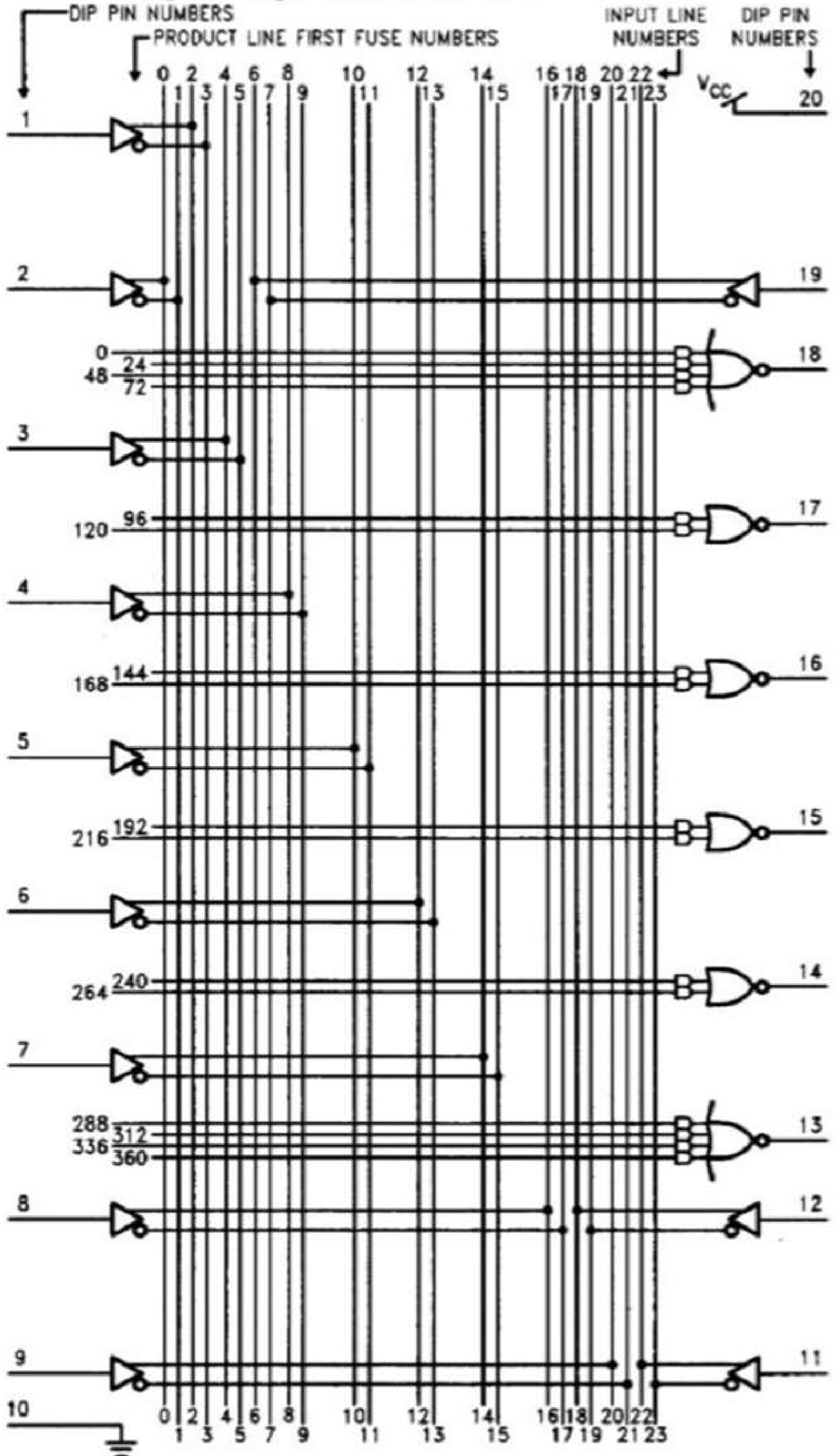
Logic Diagram PAL12L6 FDCU6



Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

Logic Diagram PAL12L6 FDCU12



Note: JEDEC Logic Array Fuse Number = Product Line First Fuse Number + Input Line Number.

FDCU6	FDCU12
1 FDCU6(13)	1 8MHz onboard clock
2 FDCU6(14)	2 A0 PEB(43)
3 TMS9901(30) INT11*/P11	3 A1 PEB(44)
4 FDCU12(14)	4 A2 PEB(41)
5 FDCU12(15)	5 A3 PEB(42)
6 FDCU12(16)	6 A4 PEB(39)
7 A12 PEB(31)	7 A5 PEB(40)
8 A15/CRUOUT PEB(30)	8 A6 PEB(37)
9 WE* PEB(54)	9 A7 PEB(38)
10 GND	10 GND
11 “1” AND A14 AND WD1773(20) [drive motor on “1”]	11 A8 PEB(35)
12 WD1773(27)	12 A9 PEB(36)
13 FDCU6(1)	13 CE* TMS9901(5)
14 FDCU6(2)	14 FDCU6(4)
15 READY PEB(4)	15 FDCU6(5)
16 2ea 8K ROM(20) CE*	16 FDCU6(6)
17 RDBENA* PEB(11)	17 NA not used
18 NA not used	18 NA not used
19 WD1773(28) [“1” command comp] [“0” status reg reset]	19 MEMEN* PEB(56)
20 VCC	20 VCC

Schematic

Name

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