

/** MMU Inputs **/

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Pin 01 = A11      : /* address bit 11      */
Pin 02 = A12      : /* address bit 12      */
Pin 03 = A13      : /* address bit 13      */
Pin 04 = A14      : /* address bit 14      */
Pin 05 = A15      : /* address bit 15      */
Pin 06 = MAP      : /* PB7 diagnostic bit  */
Pin 07 = RD4      : /* right cart. @ $8000-$9FFF */
Pin 08 = RD5      : /* left cart. @ $A000-$BFFF */
Pin 09 = REN      : /* PBO OS ram enable   */
Pin 11 = REF      : /* DRAM refresh        */
Pin 14 = MPD      : /* Math Pack Disable   */
Pin 18 = BE       : /* Basic Enable        */

```

/** MMU Outputs **/

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Pin 12 = !S5      : /* left cart. select   */
Pin 13 = !BASIC   : /* Basic ROM select    */
Pin 15 = !OS      : /* OS code select      */
Pin 16 = !CI      : /* DRAM CAS inhibit    */
Pin 17 = !IO      : /* I/O select @ $D000-$D7FF */
Pin 19 = !S4      : /* right cart. select  */

```

/** MMU Logic Equations **/

/** # is or **/
 /** ! is not **/

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S4 = !A13 & !A14 & A15 & RD4 & REF; /* RD4 and addresses $8000-$9FFF */
S5 = A13 & !A14 & A15 & RD5 & REF; /* RD5 and addresses $A000-$BFFF */

IO = A12 & !A11 & !A13 & A14 & A15 & REF; /* addresses $D000-$D7FF */

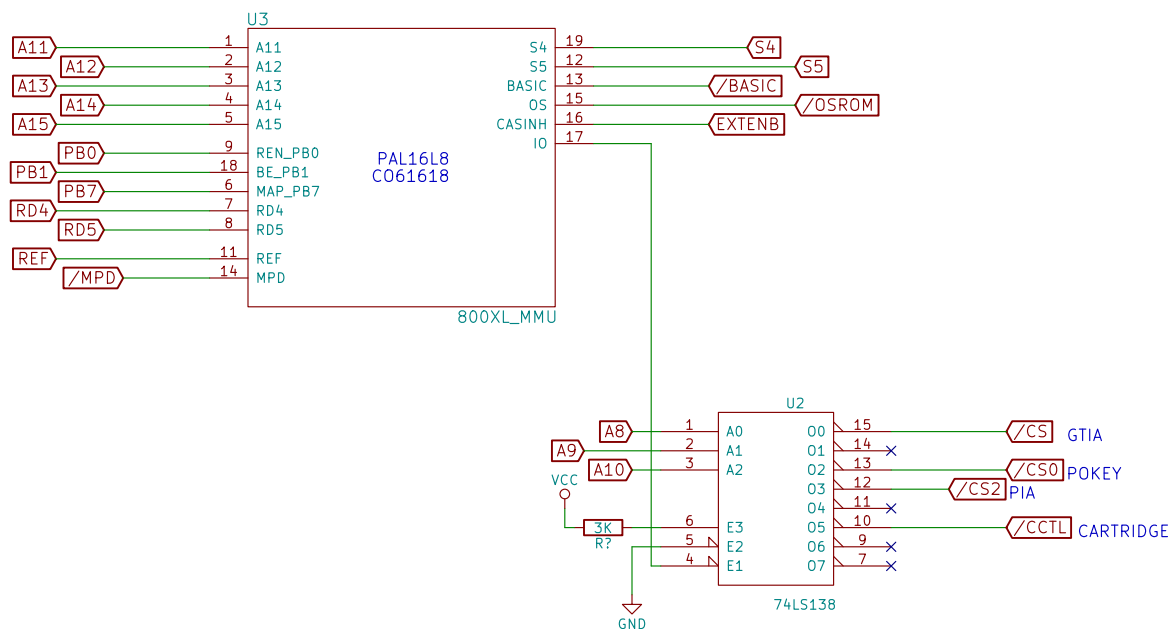
CI = !A13 & !A14 & A15 & RD4 & REF /* right cart. */
# A13 & !A14 & A15 & RD5 & REF /* left cart. */
# A13 & !BE & !A14 & A15 & !RD5 & REF /* BE and $A000-$BFFF */
# OS /* OS addresses */
# A12 & !A11 & !A13 & A14 & A15 & REF /* I/O addresses */
# !REF; /* memory refresh */

OS = A13 & A14 & A15 & REN & REF /* addresses $E000-$FFFF */
# !A12 & !A13 & A14 & A15 & REN & REF /* addresses $C000-$CFFF */
# A12 & A11 & !A13 & A14 & A15 & MPD & REN & REF /* addresses $D800-$DFFF */
# A12 & !A11 & !A13 & A14 & !A15 & !MAP & REN & REF; /* addresses $5000-$5800 - mapped */

BASIC = A13 & !BE & !A14 & A15 & !RD5 & REF; /* BE and $A000-$BFFF */

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/** from Bob Woolley, 1999FEB25 **/



D000-D0FF GTIA
 D100-D1FF PBI (unused internally)
 D200-D2FF POKEY
 D300-D3FF PIA
 D400-D4FF ANTIC
 D500-D5FF Cartridge Control
 D600-D7FF PBI (unused internally)

