OrCAD PLD COMPILER-386 V1.00 11/25/91 (Source file .\MIB3G1.PLD)

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  1  File:      MIB3G.PLD
  2  Date:      July 21, 1992
  3
  4  This file contains the logic necessary for a GAL16V8 to perform I/O
  5  Decoding for the new version of the Micro Innovations Multipurpose
  6  Interface board (MIB3)
  7
  8  Address map:
  9
 10  Duart RESET                                  1CH (Output)
 11  Duart I/O space                              10H-1FH
 12  Printer Data out                    40H
 13  Printer Status in                   40H
 14  Memory Board Bank Switching Port    42H
 15
 16  I/O Pin Definitions:
 17
 18  |GAL16V8A
 19  |  1:A0,           2:A1,           3:A2,           4:A3,
 20  |  5:A4,           6:A5,           7:A6,           8:A7,
 21  |  9:WR,           11:RD,          12:MSTB,        13:IORQ,
 22  |  14:PEN,         15:PSTB,        16:PBIN,        17:SCE,
 23  |  18:SRST,        19:PBOUT
 24
 25  Acronyms:
 26
 27     Inputs -
 28
 29     A0-A7   = Z80 Address Lines A0 - A7
 30     WR      = Z80 Write Pulse
 31     RD      = Z80 Read Pulse
 32     IORQ    = Z80 I/O Request Pulse
 33     PEN     = Parallel Printer Port Enable
 34     PBIN    = Printer BUSY line input
 35
 36     Outputs:
 37
 38     MSTB    = Memory Expansion Board Strobe
 39     SCE     = Serial I/O Chip Enable
 40     PSTB    = Printer Output Data Strobe
 41     PBOUT   = Printer BUSY line to processor (D0)
 42     SRST    = RESET line to SIO chip
 43
 44  |  High: A[0..7], PEN, PSTB, PBIN, PBOUT, SRST
 45  |
 46     Conditioning: (IORQ & RD & A[7..0]==40H & PEN) ?? PBOUT
 47  |  Conditioning: PEN ?? PSTB
 48  |
 49  |  PBOUT   = (IORQ & RD & A[7..0]==40H & PEN) ?? PBIN'
 50  |  PSTB    = IORQ & WR & A[7..0]==40H
 51  |  MSTB    = IORQ & WR & A[7..0]==42H
 52  |  SCE     = IORQ & A[7..4]==0001B
 53  |  SRST    = IORQ & WR & A[7..0]==1CH
 54  |
 55  |  Signature: "MIB3rev1"

♀I289  Complex GAL architecture selected.


RESOLVED EXPRESSIONS (Reduction 2)
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Signal name	Row	Terms
PBOUT	0	A0' A1' A2' A3' A4' A5' A6 A7' RD IORQ PEN
	1	PBIN'
PSTB	32	PEN
	33	A0' A1' A2' A3' A4' A5' A6 A7' WR IORQ
MSTB	57	A0' A1 A2' A3' A4' A5' A6 A7' WR IORQ
SCE	17	A4 A5' A6' A7' IORQ
SRST	9	A0' A1' A2 A3 A4 A5' A6' A7' WR IORQ

SIGNAL ASSIGNMENT

Pin	Signal name	Column	Rows Beg	Rows Avail	Rows Used	Activity	
1.	A0	2	-	-	-	High	(Clock)
2.	A1	0	-	-	-	High	
3.	A2	4	-	-	-	High	
4.	A3	8	-	-	-	High	
5.	A4	12	-	-	-	High	
6.	A5	16	-	-	-	High	
7.	A6	20	-	-	-	High	
8.	A7	24	-	-	-	High	
9.	WR	29	-	-	-	Low	
11.	RD	31	-	-	-	Low	(Enable)
12.	MSTB	1	56	8	1	Low	(Three-state)
13.	IORQ	27	48	8	0	Low	(Three-state)
14.	PEN	22	40	8	0	High	(Three-state)
15.	PSTB	18	32	8	2	High	(Three-state)
16.	PBIN	14	24	8	0	High	(Three-state)
17.	SCE	11	16	8	1	Low	(Three-state)
18.	SRST	6	8	8	1	High	(Three-state)
19.	PBOUT	0	0	8	2	High	(Three-state)
				64	7 (11%)		

I200 No fatal errors found in source code.
I201 No warnings.

♀OrCAD PLD-386
Type: GAL16V8A
*
QP20* QF2194* QV1024*
F0*
L0000 10 10 10 11 10 11 10 11 10 11 01 01 10 10 11 10 *
L0032 11 11 11 11 11 11 11 10 11 11 11 11 11 11 11 11 *
L0256 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0288 10 10 01 11 01 11 01 11 10 11 10 11 10 10 10 11 *
L0512 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L0544 11 11 11 11 11 11 01 11 10 11 10 11 10 10 11 11 *
L1024 11 11 11 11 11 11 11 11 11 11 11 01 11 11 11 11 *
L1056 10 10 10 11 10 11 10 11 10 11 01 11 10 10 10 11 *

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L1792 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L1824 01 10 10 11 10 11 10 11 10 11 01 11 10 10 10 11 *
L2048 11 01 11 10 01 00 11 01 01 00 10 01 01 00 00 10 *
L2080 00 11 00 11 01 11 00 10 01 10 01 01 01 11 01 10 *
L2112 00 11 00 01 11 11 11 11 11 11 11 11 11 11 11 11 *
L2144 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 11 *
L2176 11 11 11 11 11 11 11 11 11 *
C31E3*

I202  8/29/92  3:31 pm  (Saturday)
I203  Memory usage 19K
I204  Elapsed time 3 seconds

♀
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